REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated November 23, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-20 are under consideration in this application. Claims 1, 6, 10-11 and 16 is being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention.

All the amendments to the specification and the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Allowable Subject Matter

Claims 6, 9 and 16 would be allowed if they are rewritten in independent form to include the limitations of the base claim and any intervening claims.

As claims 6 and 16 are being rewritten in independent form to include the limitations of the base claim and any intervening claims, and claim 9 depends from claim 6, these claims are in condition for allowance.

Prior Art Rejections

Claims 1-5, 7-8, 10-15 and 17-20 were rejected under 35 U.S.C. § 102(a) as being anticipated by US Patent No. 6,504,739 to Phadke (hereinafter "Phadke"). Other references were cited as pertinent to the application. The above rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit of the invention for power supply control performs switching control of a switching power supply device which switches current flowing through a primary coil of a transformer TS1 for voltage conversion to drive the primary coil with alternate currents and rectifies currents flowing through a secondary coil of the transformer to output DC voltages.

The semiconductor integrated circuit (for example, the 2nd embodiment depicted in

Figs. 1 3-4, 9; pp. 11-24), as now recited in claim 1, generates and outputs a signal AD3 for dynamically controlling off-timings of a transistor (e.g., M6 or SF, p. 23, last paragraph) for synchronous rectification at the secondary coil in accordance with at least one of an input voltage Vin of the primary coil and a load current Iout of the secondary coil.

The invention of claim 11 is directed to a switching power supply device comprising: the semiconductor integrated circuit of claim 1; a transformer for voltage conversion; a switching circuit which switches currents flowing through the primary coil of the transformer for voltage conversion to drive the primary coil with alternate currents; a rectifier circuit including a synchronous rectification transistor and rectifies currents flowing through a secondary coil to output DC voltages, the synchronous rectification transistor being connected between one terminal of the secondary coil of the transformer for voltage conversion and a reference potential terminal and turned on or off in synchronization with switching operations of the switching circuit; and a capacitor element for smoothing voltages rectified by the rectifier circuit. An input voltage to the primary coil is divided by resistors and is supplied to the semiconductor integrated circuit for power supply control.

The invention recited in the claims 1 and 11 reduces power losses at a secondary side for the secondary coil, by the transistor being turned off at the optimal timing in accordance with changes in load currents at the secondary side or the input voltage of the primary coil (p. 5, 2nd paragraph; p. 6, last 2 paragraphs; p. 24, last paragraph).

The semiconductor integrated circuit (for example, the 2nd embodiment depicted in Fig. 15 & Figs. 16(3)-(4); pp. 34-39), as now recited in claim 10, is configured to selectively set any detection criterion level VBS (Fig. 15) for a circuit to generate a signal (e.g., OUT-B) which detects a voltage between terminals of a switching element (e.g., M2) in a circuit for switching currents flowing through the primary coil and controls on-timings.

The invention recited in the claim 10 reduces power losses of a primary side for the primary coil by being able to set any detection criterion level (p.5, 3rd paragraph; p. 7, 2nd & 3rd paragraphs).

Applicants contend that Phadke fails to teach or suggest (1) "generating and outputting a signal AD3 for dynamically controlling off-timings of a transistor for synchronous rectification at the secondary coil in accordance with at least one of an input voltage Vin of the primary coil and a load current Iout of the secondary coil" (Claims 1 and 11); or (2) "selectively setting any detection criterion level for a circuit to generate a signal which detects a voltage between terminals of a switching element in a circuit for switching

currents flowing through the primary coil and controls on-timings" (Claim 10) so as to minimize switching power losses according to the invention.

In contrast, Phadke merely drives both synchronous rectifiers Q1, Q2 to an on state during a dead time period of operation. The onset of the dead time period occurs when the diagonal conducting switching device is driven to an off state, and drives the second of the two synchronous rectifiers Q2 to an on state only after one of the diagonal switching devices has been driven to an off state by the primary control circuit, so as to eliminate the risk of cross conduction between the synchronous rectifiers (Abstract), rather than to minimize switching power losses as does the invention.

Phadke (Fig. 5) simply does not (1) "generate and output a signal AD3 for dynamically controlling off-timings of a transistor for synchronous rectification at the secondary coil in accordance with at least one of an input voltage Vin of the primary coil and a load current Iout of the secondary coil"; nor (2) "selectively set any detection criterion level for a circuit to generate a signal which detects a voltage between terminals of a switching element in a circuit for switching currents flowing through the primary coil and controls on-timings" so as to minimize switching power losses according to the invention.

Applicants contend that the cited references or their combinations fail to teach or disclose each and every feature of the present invention as disclosed in the independent claims 1 and 10-11. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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